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INVERTER FOR USE WITH VERY LOW INPUT VOLTAGES

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Thomas G. Wilson Edward T. Moore

A continuing impetus to advance the technology of static energy-conversion methods is being provided by the demands of our and other nations' rapidly expanding programs of space exploration. Not only the various environmental considerations, but more particularly, the stringent reliability requirements serve to justify the considerable research effort being directed toward the development of static methods for the generation and processing of electrical energy for spacecraft.

Considerable interest, stemming not only from the space effort but also from concern over our rapidly depleting sources of fossil fuels (1), is presently being focused on a variety of new sources of electrical energy. Fuel cells, thermionic diodes, thermoelectric generators, and solar cells are presently being used and planned for many additional uses in a variety of isolated electrical power systems. Though these devices differ in many respects, they share one important common characteristic: they provide a direct-current output at a very low voltage level. Thus, if these sources are to be used to provide power to a d-c to a-c inverter or a d-c to d-c converter, either enough of the low voltage generators must be connected in series so that the input voltage to the converter may be raised to a level which will enable the converter to perform efficiently, or the converter must be capable of efficient performance with a very low-voltage high-current input. The latter alternative, minimizing the number of generators connected in series, is definitely the more attractive from the viewpoint of reliability.

It is the purpose of this paper to consider some of the problems involved in designing transistorized converters for use with low-voltage supplies and to describe a d-c to a-c inverter which is particularly well suited for operation with a very low-voltage input. This circuit also enables greater advantage to be taken of the potential efficiency of the transistor switches despite wide variations in the magnitude of the input voltage to the converter and in the load current drawn by the converter. Finally, a test circuit is described whose performance is illustrative of the efficiency and other characteristics of this type of inverter.

BACKGROUND

Insofar as the necessary size and weight of the magnetic components of an inverter for a given power and frequency are concerned, the level of the input voltage to the inverter is of little consequence. It is largely the limitations imposed by the saturated voltage drop of available static switching elements that establish the lowest practical input-voltage level at which the inverter may be operated. A number of switching elements, including tunnel diodes, have been considered.(2,3) Particular attention

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is being given today to the use of transistors for this purpose, (2,4) and several transistor manufacturers have recently developed special transistors with this application in mind.

The actual degree to which the potential efficiency of a transistor switching element is actually realized in an inverter depends on many factors other than the transistor itself. In particular, many of the switching-transistor inverter circuits which, because of their simplicity and reliability, have been widely used in the past are not well suited for low-voltage applications in which minimizing the losses in the switching elements becomes of critical importance. Several reasons for this are mentioned briefly below.

A self-oscillating inverter utilizing a saturable core and a pair of switching transistors was proposed by Royer in 1955 (5). Since that time, this circuit has been thoroughly discussed in the literature, and a great many other magnetically coupled multivibrators involving the same general principles have been proposed (5-9). These inverter circuits have often been used in d-c to d-c converters and are particularly well suited for this application involving rectification and filtering because of their square-wave output voltage.

Familiarity on the part of the reader with the circuit of Reference 5 and with the operating principles involved in this general class of circuits is assumed. Therefore, the discussion of such circuits will be limited to pointing out two things about their operation which are of particular importance when considering efficiency.

The first of these is that the magnitude of the base current supplied to the transistors in this class of inverters is a function of the input voltage to the inverter rather than of the transistor collector current. Thus, the design of such an inverter must insure that, under conditions of minimum input voltage, the base current to a conducting transistor is sufficient to maintain the transistor in the saturated state when the load current is a maximum. If such an inverter is to be operated over a range of input voltages, it is necessary that a resistor be placed in the transistor base circuits to limit the base current during those times that the input voltage to the inverter is high. This means that the total power dissipated in the transistor base circuits involves not only the emitter-base junction dissipation within the transistors but also the dissipation in the added base-circuit resistance.

If the input voltage variation is wide, this latter loss often significantly exceeds the internal loss across the junction. Furthermore, because the base current is a function of the input voltage rather than of the load current, the transistor base drive will remain at a value corresponding to maximum-load conditions even though the inverter may be operated at much less than maximum load for long intervals of time. Clearly the transistors would be used more optimally if the resistor in the base circuit could be eliminated and if the transistor base current were always proportional to the collector current and independent of the input voltage to the inverter.

A second efficiency-limiting characteristic is that each switching action of the inverter transistors is preceded by and, in fact, is actually initiated by a large collector-current surge in the transistor whose conducting half cycle is ending. This cyclic current surge itself represents a loss. It also indirectly further adversely affects the inverter efficiency

by causing the dissipation within the transistor during the switching interval to be increased. This is brought about because a large surge of current through a transistor just prior to its emitter-base junction being reverse-biased tends to increase its storage and decay times and therefore to increase its switching losses (10).

TRANSISTORS AS LOW VOLTAGE SWITCHES

Although it is not the purpose of this paper to examine in detail the characteristics of switching transistors, the following discussion points out the fact that, in very-low-voltage circuits, transistors may become quite inefficient switching elements.

The power dissipation occuring in a transistor while it conducts may be subdivided into two parts, P_B and P_{CE}. P_B is the base-drive power used to hold the transistor in the saturated state and P_{CE} is the power dissipation given by the product of the collector current and the collector-to-emitter voltage. These may be expressed as

$$P_B = V_{BE} I_C/K$$

$$P_{CE} = V_{CE} I_C$$

where V_{BE} = voltage from base to emitter, V_{CE} = voltage from collector to emitter, I_C = collector current, and K = ratio of collector current to base current. (K has been used here rather than h_{FE} because in most applications more base current intentionally will be supplied to the transistor than the minimum amount required to keep the transistor saturated.)

Both P_B and P_{CE} increase with increasing collector current and are independent of the input voltage E_{in} supplied to the circuit. For a given current I_C these two losses establish a certain minimum input voltage below which the efficiency of the transistor as a power-controlling element becomes zero. Using previously defined symbols, an upper limit of the efficiency of the transistor can be expressed as

$$\text{Eff.} = \frac{E_{in}I_C - (P_B + P_{CE})}{E_{in}I_C} = \frac{E_{in}I_C - \left(\frac{V_{BE}I_C}{K} + V_{CE}I_C\right)}{E_{in}I_C} \qquad (1)$$

For the value of E_{in} at which $E_{in} = (P_B + P_{CE})/I_C$ the transistor efficiency is zero, i.e. none of the input power can be delivered to a load and is instead completely absorbed by the transistor itself.

In a circuit in which the transistor is cyclically switched on and off the actual transistor efficiency will always be somewhat lower than the upper limit defined by Equation (1). This is because there is a slight power dissipation within the transistor in the nonconducting state and, more importantly, because the transistor is cyclically subjected to brief periods of high dissipation during the switching intervals. In general though, the dissipation in a transistor in the nonconducting state with the emitter-base junction reverse biased is insignificant in comparison to the other losses. On the other hand, the power dissipated during the transient switching intervals may become quite significant and will depend on the type of transistor and the characteristics and frequency of the

particular inverter circuit used. Transistors having relatively low resistivities such as are necessary for low-voltage high-current applications usually are characterized by relatively long storage and decay times and, therefore, by high switching losses when used in a relatively high-frequency inverter. So that the transistor storage and delay times are not unduly lengthened, it is very desirable to take steps to insure that no surge of collector current precedes each switching action. Such a cyclic pulse of current is, however, a characteristic of many commonly employed inverter circuits.

From the above discussion it should be evident that transistors are not necessarily always able to perform as efficient switching elements, and that this is especially true insofar as their use in very-low-voltage inverters is concerned.

Curve A of Figure (3) is a plot of Equation (1) showing efficiency versus input voltage for a transistor with the following characteristics: V_{BE} = 0.60 volts, V_{CE} = 0.020 volts, and K = 10. The current I_C is assumed constant at 20 amperes. This curve does not include all the losses within a transistor used in a switching circuit so consequently it simply represents an upper limit to the power-controlling efficiency of the transistor which can be approached in practice but can never actually be realized. The reason for assuming the particular set of characteristics used for plotting Curve A of Figure (3) is that they correspond very closely to the characteristics exhibited by the transistors used in the test circuit to be discussed in a later section. Curve A of Figure (3) will be compared to the actual overall-efficiency versus input-voltage curve of the test circuit as a measure of the degree to which the inverter of this paper approaches optimum use of the transistors.

DESCRIPTION OF CURRENT-FEEDBACK INVERTER

The preceding discussion has emphasized the fact that the losses within a transistor become particularly significant when the transistor is to be used as a switching element in a low-voltage circuit such as an inverter. In low-voltage circuits, the manner in which base current is provided to the transistors becomes especially important.

Figure 1 is the circuit of a d-c to a-c inverter which is self-oscillating and in which the feedback to the transistor switching elements involves proportionality between the collector currents and base currents on an instantaneous basis. With this inverter, even though the input voltage varies, or the load current varies, or even in applications in which the transistor collector currents vary over a wide range within each half cycle as, for example, when the inverter output is rectified and passed through certain types of regulators and filters, the ratio of the collector current to the base current of each transistor remains constant at a predetermined value established in accordance with the requirements of the transistor. As is seen from the figure, a high degree of simplicity is displayed by the circuit.

Theory of Operation

The operation of this circuit depends on the combined effects of three nonlinear characteristics: (1) the current-voltage characteristic of the rectifying emitter-base junction of the transistors, (2) the current-voltage characteristics between the collector and emitter terminals of the transistors, and (3) the hysteresis loop of core T_2. Transformer T_1

serves merely as the output transformer for the inverter. Normally core T_1 never becomes saturated although, as will be seen, the characteristics of core T_1 near saturation can have some effect on the operation of this inverter.

As in other parallel inverters, the two transistors of this inverter are alternately turned on and off so as to impress the input voltage E_{in} first across N_1 and then across N_2 of the output transformer, thereby inducing a square wave of alternating voltage in the output winding N_3. Switching of the transistors is caused by the cyclic saturation of the square-loop core T_2, but not in such a manner as to be accompanied by a surge of current through the transistors.

Core T_2 will ordinarily have a physical size and cross-sectional area which is very small compared to that of core T_1. Core T_2 and its windings can best be thought of as a sharply-saturable current transformer. With one transistor conducting and transformer T_2 unsaturated, the load impedance limits the transistor collector current, and the base current is dictated by the turns ratio $N_4/N_5 = N_7/N_6$ of the current transformer. For any particular inverter, this ratio is chosen in accordance with the base-drive requirements of the transistors.

If, for example, transistor Q_1 is conducting with given values of collector and base currents, its emitter-to-base voltage drop appears across winding N_5 and this voltage drop establishes the rate-of-change of flux in core T_2. Ultimately, however, T_2 becomes saturated and decoupling takes place between windings N_4 and N_5. The base current to transistor Q_1 then decreases and Q_1 is turned off. Some energy is stored in the after-saturation inductance of core T_2 and, as this energy is returned to the circuit, transistor Q_2 is turned on. The circuit is self-oscillating and is symmetrical with events in alternate half cycles being complementary.

Figure 2 provides more detailed insight into the functioning of the inverter. In Figure 2(A), the magnetomotive forces (mmf's) resulting from the currents in the individual windings on core T_2 are plotted as a function of time throughout one cycle. Because of the rectifying action of the transistor junctions, bi-directional current flow is not possible in any of the windings on core T_2. Thus the mmf's N_4I_C and N_6I_B always tend to magnetize the core positively whereas N_5I_B and N_7I_C always tend to magnetize the core negatively. During a given half cycle, the net mmf applied to the core is either $(N_4I_C - N_5I_B)$ or $(N_7I_C - N_6I_B)$. The variation of this net mmf (ΣNI) through one complete cycle is shown as a function of time in Figure 2(B). In Figure 2(C) the variation in the magnitude of this net mmf is related to the flux level ϕ in the core.

At points A on the curves of Figure 2(A), (B) and (C), transistor Q_1 has just been turned on and core T_2 is at its negative saturation-flux level. The load impedance limits the current I_C. The base current I_B is proportional to I_C, with N_4/N_5 being the constant of proportionality. The emitter-to-base voltage drop of transistor Q_1 appears across winding N_5 and this establishes the rate of change of flux in core T_2. The difference $(N_4I_C - N_5I_B)$ of the two mmf's applied to core T_2 is equal to the magnetizing mmf of core T_2 and remains small and relatively constant as the flux in the core moves from the negative toward the positive saturation-flux level. At points B on the plots of Figure 2, core T_2 begins to saturate and the mmf required to allow further flux change in the positive direction begins to increase rapidly. The current I_C in winding N_4 is limited by the load

impedance and so cannot increase as T_2 begins to saturate. Instead, the current I_B in winding N_5 decreases as core T_2 saturates.

At points C in Figure 2, the base current I_B has dropped to a value such that $(I_C/I_B) = h_{FE}$ where h_{FE} is the maximum ratio of collector to base current at which the transistor can remain saturated. Thus, at points C, Q_1 begins to become unsaturated and its emitter-to-collector voltage begins to increase rapidly. The voltage applied to the load and the current I_C therefore begin to decrease. As the apparent resistance of Q_1 increases, the net mmf applied to core T_2 reaches a maximum at point D on the curves and thereafter begins to decrease. In accordance with the magnetic characteristics of the core, this decrease in mmf implies a reversal of the direction of flux movement within core T_2 and a reversal in polarity of the voltages induced in windings N_5 and N_6. A forward voltage therefore appears across the emitter-base junction of Q_2 and this transistor begins to conduct. At the same time, the emitter-base junction of Q_1 becomes reverse-biased and this transistor rapidly ceases to conduct. At points E, all of the energy stored in the after-saturation inductance of core T_2 as it was driven into saturation has been returned to the circuit. Transistor Q_1 has been turned off, transistor Q_2 has been turned on, and a new half cycle has been initiated.

Frequency of Oscillation

The frequency of oscillation f is given by the following relation

$$f = \frac{V_{BE}}{4NAB_m} 10^8 \qquad (2)$$

where $N = N_5 = N_6$, A = the cross-sectional area of core T_2 in square-centimeters, and B_m = saturation flux density of core T_2 in gauss. The voltage V_{BE} of the emitter-base junction is a function of the base current I_B, and therefore is actually a function of the load current drawn from the inverter. As the transistor base currents are increased, the inverter frequency increases in accordance with the diode-like V-I characteristics of the emitter-base junctions of the transistors.

Effect of Transistor Mismatch

It is possible that with equal base currents a given pair of transistors may exhibit unequal forward emitter-base voltage drops. Such a situation is clearly of potential significance in this inverter since it is the emitter-base voltage drops of the transistors which determines the length of each half cycle. Placing a resistor in series with the bases of the transistors such that the voltage drop across the resistor becomes large with respect to the emitter-base voltage drop is, of course, an obvious way of obscuring any transistor mismatch which might exist. However, in so doing, an efficiency penalty is paid, and this loss in efficiency becomes especially important in low-input-voltage situations. Thus, it is worthwhile to consider in some detail the possible implications of mismatched transistors in this inverter when no base resistance is added.

A mismatch in which, for example, the emitter-base voltage drop of Q_1 is greater than that of Q_2 results in a higher voltage appearing across winding N_5 during the half cycles in which transistor Q_1 conducts than appears across N_6 during the alternate half cycles. The conduction interval

of Q_1, in such a case, tends to be slightly shorter than that of Q_2. Since the magnitudes of the voltages applied to windings N_1 and N_2 on core T_1 are equal, core T_1 is driven slightly into saturation at the end of each half cycle during which Q_2 is the conducting transistor. As core T_1 becomes even slightly saturated, its magnetizing current increases and therefore the collector current I_C is increased. This increased collector current produces an increased base current which in turn produces an increased emitter-base voltage drop in transistor Q_2. This forced increase in the emitter-base voltage of Q_2 compensates for the unbalance between the two inverter transistors and tends to make the lengths of alternate half cycles equal.

A potentially troublesome situation may exist when two highly dissimilar transistors are used and no base resistance is added. For example, if core T_1 has a highly square hysteresis loop and if the degree of unbalance between the two transistors is large, core T_1 may be driven rather significantly into saturation on alternate half cycles and the resulting surges of collector and base current may then become large and may be expected to cause heating of the transistor with the lower emitter-base voltage drop. The emitter-base voltage drop of a transistor is itself temperature dependant and so the degree of mismatch between the emitter-base voltages of the two transistors will be affected by heating of one transistor. The temperature dependence of the emitter-base voltage of a transistor is rather involved (11). If, as would usually be expected, this heating causes the emitter-base voltage to decrease, this will aggravate the mismatch which originally existed between the two transistors. In this manner, it is possible under certain circumstances that the circuit operation may become so unsymmetrical as not only to impair its efficiency but also to cause undue heating and potential failure of one transistor.

Actual experience with this inverter circuit using a variety of transistors operating at various current and voltage levels indicates that by using reasonable discretion this inverter is quite readily operated without the need for any base-circuit resistance. Among the measures that may be used to insure against the type of situation described in the preceding paragraph are the selection of transistors with reasonably well matched characteristics and the mounting of these transistors in close proximity on a common heat sink. Finally, it should be noted that even a rather serious degree of mismatch between the emitter-base voltage drops of the two transistors can be compensated for in a relatively easy manner by adjusting the relative number of turns in windings N_5 and N_6. For example, by adding a small percentage of turns to the base winding corresponding to the transistor having the higher emitter-base drop, the volts per turn appearing on these windings may be equalized despite unequal voltages existing because of a transistor mismatch. This, in fact, was done for the test circuit whose performance is described in the next section.

TEST CIRCUIT PERFORMANCE

The particular low-voltage converter whose performance is described here has been designed to accept input voltages ranging from 0.5 volts to 4.0 volts. In designing this inverter for such a wide input-voltage range, some efficiency was necessarily sacrificed in the 0.5 to 1.0 volt range because of the losses associated with the surplus capacity of the output transformer at these levels. However, this test circuit illustrates rather well the ability of such an inverter to perform efficiently under a diversity of input-voltage and load conditions.

The components of the test circuit are described in Table 1. With an input current of 20 amperes this inverter oscillates at a frequency of approximately 650 cycles per second. The alternating output voltage is essentially a square wave. At an input current of 30 amperes very little heating of the inverter transistors was noted. No problems of thermal instability existed with this test circuit. The inverter was not always self-starting, however, and for test purposes in the laboratory, oscillations were initiated by momentarily connecting a one-ohm resistor from the emitter of one transistor to its collector. As in other types of magnetically coupled multivibrators, the addition of simple provisions to insure spontaneous starting should present little difficulty.

Table 1

Q_1, Q_2	Motorola XP726
T_2	ID = 1.08, OD = 1.26, H = 0.08 in., Magnetics, Inc., No. 51395-2A
T_1	ID = 1.5, OD = 2.5, H = 0.5 in., Magnetics, Inc., No. 52001-4A
$N_4 = N_7$	5 turns of 15 strands of #18 wire
N_5	49 turns of #18 wire
N_6	50 turns of #18 wire
$N_1 = N_2$	10 turns of 15 strands of #18 wire
N_3 =	192 turns of #18 wire
Load	Resistive

The input power to this test circuit was supplied from an essentially ripple-free source of direct current. For the purpose of efficiency determinations, the true rms value of the inverter output voltage as applied to calibrated resistive loads was measured. The output power computed as V^2/R was then compared to the input power as determined by the product of the average input current and input voltage.

Curve B of Figure 3 shows the measured overall efficiency of the inverter from zero to three volts, with a constant average input current of 20 amperes. Curve A, which has been previously mentioned, is a plot of the upper limit of the theoretically possible inverter efficiency taking into account only the losses occurring in the transistors themselves during their intervals of saturated conduction. A comparison of curves A and B provides some indication of the degree to which the utilization of the transistors of this inverter approaches the limits dictated by the transistors themselves. In comparing these two curves it should be remembered that curve A takes into account only the conduction losses of the transistors, whereas curve B reflects not only the effects of these conduction losses but also the additional switching-interval transistor losses, and the core and copper losses of the inverter transformers. The inverter efficiency is seen to be very high, increasing from 79.0% at 1 volt input to 93.6% at 3 volts input. At the 3-volt input level, the measured circuit efficiency is only 3.7% less than the upper limit computed using Equation (1).

The two curves of Figure 4 show the manner in which the measured efficiency varies as the input current to the inverter is varied over a wide range. In the upper curve, the input voltage to the inverter was held constant at 3 volts. The efficiency showed very little variation, remaining above 90% as the current was varied from 5 to 30 amperes. In the

lower curve, for which the input voltage was 1.0 volts, this same 5 to 30 ampere variation of the input current caused greater variation in the efficiency. This is to be expected in view of the increased significance of the transistor limitations and the I^2R losses in the transformer windings at this lower voltage. In accordance with the current-proportional feedback made possible by the use of the saturable current transformer, these two curves indicate a high efficiency throughout a wide range of loads.

CONCLUSIONS

Insofar as the necessary size and weight of the magnetic components of an inverter for a given power and frequency are concerned, the level of the input voltage to the inverter is of little consequence. It is largely the limitations imposed by the available static switching elements that establish the lowest practical input voltage level at which the inverter may be operated. Transistors specially designed for high-current low-voltage circuits represent one of the best types of switching elements available for low voltage inverters and have characteristics which indicate potentially high efficiency for **this** application. However, the degree to which the potential efficiency of a transistor switching element is actually realized in an inverter depends on many factors other than the transistor itself. In particular, in very-low-voltage circuits, the dissipation involved in supplying the transistor with adequate base drive under all conditions becomes especially significant.

In the switching-transistor inverter described in this paper, the transistors are used in a near-optimum manner despite the fact that the inverter may be subjected to widely varying input voltages and load conditions. Moreover, this is achieved in a circuit having a minimum of complexity. Feedback is provided to the inverter transistors through a nonlinear current transformer such that, regardless of the level of the load current or input voltage, the transistor base-current to collector-current ratio is held constant. Measurements made on test circuits in the 0.2 to 3.0 volt range indicate that the efficiency of the inverter closely parallels the maximum which would be expected in view of the characteristics of the transistors themselves. With 3 volts input, an overall efficiency of 93% was obtained.

Some of the more important characteristics of this inverter are as follows:

1. The alternating voltage output is a square wave and therefore is well suited for applications requiring rectification and filtering to provide a direct voltage output.
2. A very high conversion efficiency is obtained despite wide variations in the load current or input voltage.
3. Switching of the transistors at the end of each half cycle is initiated in a manner which does not involve a surge of collector current during or just prior to the switching interval.
4. The base current delivered to each transistor is always proportional to the collector current of the transistor. This is not only very significant insofar as efficiency is concerned but also enables the inverter to withstand rather high overloads for short intervals of time without transistor damage.

A disadvantage of this inverter is the fact that within the circuit itself there is no inherent protection against the effects of a short circuit at the output terminals. If protection is to be obtained, it must be obtained through externally added protective provisions.

Attention has been focused in this paper primarily on the fact that this inverter is particularly well suited for the efficient conversion of electrical energy obtained from very low-voltage direct-current sources. This capability is especially important in view of the rapid development of a variety of new methods for the generation of electrical energy since almost all of these new sources of electrical energy are characterized by a very low-voltage direct-current output. However, it should be recognized that this inverter also is suited for use with high as well as low input voltages and that many of the same advantages are apparent in either case.

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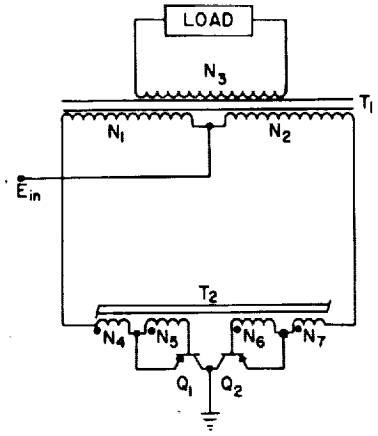

Fig. 1. Circuit of low-voltage current-feedback inverter

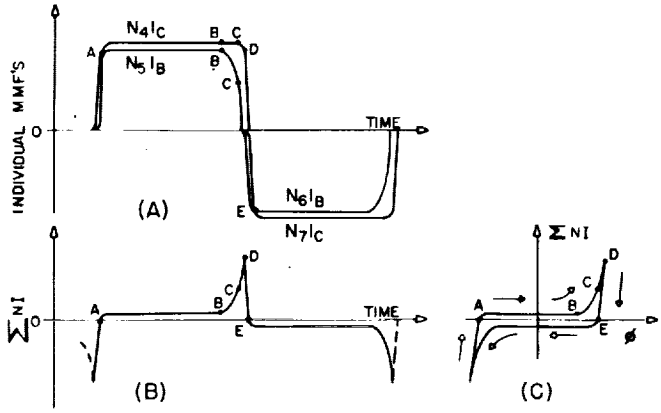

Fig. 2. Magnetomotive forces acting on core T_2
(A) Time variation of individual mmf's
(B) Time variation of net mmf
(C) Relation of net mmf to flux for core T_2

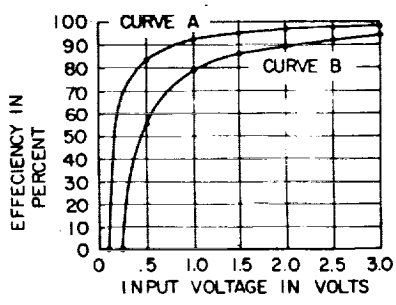

Fig. 3. Variation of efficiency with input voltage
Curve A - Calculated transistor upper efficiency limit
Curve B - Measured overall inverter efficiency

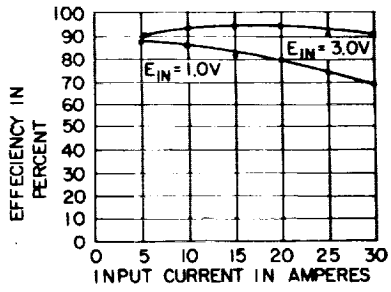

Fig. 4. Variation of inverter efficiency with input current